SELF-COMPENSATING DELAY CHAIN FOR MULTIPLE-DATE-RATE INTERFACES

ABSTRACT OF THE DISCLOSURE

Methods and apparatus for delaying a clock signal for a multiple-data-rate interface. An apparatus provides an integrated circuit including a frequency divider configured to receive a first clock signal and a first variable-delay block configured to receive an output from the frequency divider. Also included is a phase detector configured to receive the first clock signal and an output from the first variable-delay block, and an up/down counter configured to receive an output from the phase detector. A second variable-delay block is configured to receive a second clock signal and a plurality of flip-flops are configured to receive an output from the second variable-delay block. The first variable-delay block and the second variable-delay block are configured to receive an output from the up/down counter.